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10/561,870	12/21/2005	Yoshitoshi Kida	SON-3055	1396

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,870	KIDA ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/26/10, 11/4/09, 6/16/09*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *2,6 and 9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7,8 and 10-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings were received on *4 November 2009*. These drawings are acceptable.

Election/Restrictions

3. Applicant's election with traverse of ***Species I-A (Claims 1, 3, 4, 5, 7, 8, and 10-16)*** in the reply filed on *26 February 2010* is acknowledged.

The traversal is on the ground(s) that, "*the Restriction Requirement fails to establish that the special technical feature of the application is known, and thus fails to establish lack of unity of invention... Thus, there is lack of unity if it can be established that the claimed technical feature is not a special technical feature that defines a contribution over the prior art. Yet the Restriction Requirement and fails to establish that the special technical features of claim 1 are known*" (pages 8-9 of the *26 February 2010* Election). This is not found persuasive.

As demonstrated by the prior art references cited in this Office action, at least one independent claim of the application does not avoid the prior art, therefore, the special technical feature of the application is anticipated by or obvious in view of the prior art. Consequently, the inventions listed in the Restriction Requirement (*mailed on 1 February 2010*) do not relate to a single general inventive concept under PCT Rule 13.1.

Moreover, there is a search and/or examination burden for the patentably distinct species because at least the following reason(s) apply: the species or groupings of patentably indistinct species require a different field of search (e.g., searching different classes /subclasses or electronic resources, or employing different search strategies or search queries).

The requirement is still deemed proper and is therefore made FINAL.

4. ***Claims 6 and 9 are withdrawn*** from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on *26 February 2010*. As a courtesy to the Applicant, this Office action provides a rejection of *claims 6 and 9*. However, going forward *claims 6 and 9* should be treated as being withdrawn.

5. This application contains *claims 6 and 9* drawn to an invention nonelected with traverse in the reply filed on *26 February 2010*. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. *Claims 1, 3, 4, 5, 7, 8, and 10-16* (*and claims 6 and 9*) are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***transferring a first latch result of said first latch section to a second latch section***" (*line 2*) and "***transferring only an inverted output of said first latch result to said second latch section***" (*line 4*).

It would be unclear to one having ordinary skill in the art how the claimed invention is capable of "***transferring only an inverted output of said first latch result***" while also simultaneously "***transferring a first latch result***." Are both transferred, or only one?

10. Claim 1 recites the limitation "***said second latching section***" (*line 10*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art whether this limitation is intended to be identical to, or distinct from, the earlier recited "*second latch section*" (*line 2*).

11. The term "***sufficiently higher***" in claim 3 (*line 2*) is a relative term which renders the claim indefinite. The term "***sufficiently higher***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It would be unclear to one having ordinary skill in the art how much "*higher*" qualifies as "***sufficiently higher***."

12. Claim 3 recites the limitation "***reduce a voltage drop***" (*line 2*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art what such a "*voltage drop*" is *reduced* relative to. Compared to what?

13. Claim 3 recites the limitation "***said first latch***" (*line 3*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art whether this limitation is intended to be identical to, or distinct from, the earlier recited "*first latch section*."

14. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***a transfer of said first latch to said second latch section by only an inverted output***" (*claim 3, line 3*); "***transferring a first latch result of said first latch section to a second latch section***" (*claim 1, line 2*) and "***transferring only an inverted output of said first latch result to said second latch section***" (*claim 1, line 4*).

It would be unclear to one having ordinary skill in the art how the claimed invention is capable of "***transferring only an inverted output of said first latch result***" while also simultaneously "***transferring a first latch result***" and another "***inverted output***." Are they all transferred, or only one?

15. Claim 4 provides for the "***use of a single phase***," (*line 5*) but, since the claim does not set forth any steps involved in this method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

16. Claim 4 recites the limitation "***said second latching section***" (*line 10*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art whether this limitation is intended to be identical to, or distinct from, the earlier recited "*second latch section*" (*line 3*).

17. Claim 5 provides for the "***use of an inverted output of the first latch result***," (*line 2*) but, since the claim does not set forth any steps involved in this method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

18. Claim 6 provides for the "***use of a non-inverted output of the first latch result***," (*line 2*) but, since the claim does not set forth any steps involved in this method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

19. The term "***sufficiently higher***" (*line 2*) in claim 7 is a relative term which renders the claim indefinite. The term "***sufficiently higher***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It would be unclear to one having ordinary skill in the art how much "*higher*" qualifies as "***sufficiently higher***."

20. Claim 7 recites the limitation "***reduce a voltage drop***" (*line 2*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art what such a "*voltage drop*" is *reduced* relative to. Compared to what?

21. Claim 7 recites the limitation "***the transfer of said first latch result to said second latch section***" (*lines 2-3*). There is insufficient antecedent basis for this limitation in the claim.

22. The term "***sufficiently higher***" (*line 2*) in claim 8 is a relative term which renders the claim indefinite. The term "***sufficiently higher***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It would be unclear to one having ordinary skill in the art how much "*higher*" qualifies as "***sufficiently higher***."

23. Claim 8 recites the limitation "***reduce a voltage drop***" (*line 2*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art what such a "*voltage drop*" is *reduced* relative to. Compared to what?

24. Claim 8 recites the limitation "***the transfer of said first latch result to said second latch section***" (*lines 2-3*). There is insufficient antecedent basis for this limitation in the claim.

25. The term "***sufficiently higher***" (*line 2*) in claim 9 is a relative term which renders the claim indefinite. The term "***sufficiently higher***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It would be unclear to one having ordinary skill in the art how much "*higher*" qualifies as "***sufficiently higher***."

26. Claim 9 recites the limitation "***reduce a voltage drop***" (*line 2*). There is insufficient antecedent basis for this limitation in the claim.

It would be unclear to one having ordinary skill in the art what such a "*voltage drop*" is *reduced* relative to. Compared to what?

27. Claim 9 recites the limitation "***the transfer of said first latch result to said second latch section***" (*lines 2-3*). There is insufficient antecedent basis for this limitation in the claim.

28. The term "***a second inverted***" in claim 11 (*line 2*) renders the claim indefinite. It would be unclear to one having ordinary skill in the art what earlier claimed element, if any, is intended to be inverted.

29. Claim 11 recites the limitation "***said first and second inverters***" (*line 2*). There is insufficient antecedent basis for this limitation in the claim.

30. Claim 11 recites the limitation "***said power supply voltage***" (*lines 2-3*). There is insufficient antecedent basis for this limitation in the claim.

31. Claim 15 recites the limitation "***a third inverter***" (*line 3*). There is insufficient antecedent basis for this limitation in the claim. It would be unclear to an artisan whether "*first and second inverters*" are required elements of the claimed invention.

32. The term "***a fourth inverted***" in claim 15 (*line 2*) renders the claim indefinite. It would be unclear to one having ordinary skill in the art what earlier claimed element, if any, is intended to be inverted.

33. Claim 15 recites the limitation "***said third and fourth inverters***" (*line 2*). There is insufficient antecedent basis for this limitation in the claim.

34. Claim 15 recites the limitation "***said power supply voltage***" (*line 3*). There is insufficient antecedent basis for this limitation in the claim.

35. Claim 15 recites the limitation "***a second negative power supply***" (*line 3*). There is insufficient antecedent basis for this limitation in the claim. It would be unclear to an artisan whether a "*first negative power supply*" is a required element of the claimed invention.

36. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

An omitted structural cooperative relationship results from the claimed subject matter: "***said first latch result is inputted to said third inverter***" (*claim 15, line 5*) and "***said transfer by use of a single phase is carried out by use of an inverted output of the first latch result***" (*claim 5, line 2*).

It would be unclear to one having ordinary skill in the art how the claimed invention is capable of transferring "***an inverted output of the first latch result***" while also simultaneously transferring "***said first latch result***." Are both transferred, or only one?

37. Claim 15 recites the limitation "***the output of said third inverter***" (*line 5*). There is insufficient antecedent basis for this limitation in the claim.

38. The remaining claims are rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claims.

39. The claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

As a courtesy to the Applicant, the examiner has attempted to also make rejections over prior art -- based on the examiner's best guess interpretations of the invention that the Applicant is intending to claim.

However, the indefinite nature of the claimed subject matter naturally hinders the Office's ability to search and examine the application.

Any instantly distinguishing features and subject matter that the Applicant considers to be absent from the cited prior art is more than likely a result of the indefinite nature of the claims.

The Applicant is respectfully requested to correct the indefinite nature of the claims, which should going forward result in a more precise search and examination.

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

41. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

42. *Claims 1, 3, 4, 5, 7, 8, and 10-16* (*and claims 6 and 9*) are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Nakajima et al (EP 1 014 334 A2)*** in view of ***Azami et al (US 2003/0011584 A1)***.

Please note claim order has been rearranged to better reflect claim dependencies.

Regarding claim 1, ***Nakajima*** discloses a data transfer circuit [*e.g., Figs. 1, 23: 122 + 123*] for latching an input data [*e.g., Fig. 21: in1*] in a first latch section [*e.g., Figs. 1, 23: 122; Fig. 21*],

transferring a first latch result [*e.g., Fig. 21: xout = Fig. 26: in1*] of said first latch section to a second latch section [*e.g., Figs. 1, 23: 123; Fig. 26*], and

latching said first latch result in said second latch section (*e.g., see Fig. 27*), characterized by:

transferring only an inverted [*e.g., Fig. 21: via 114*] output of said first latch result to said second latch section (*e.g., see Paragraphs 147, 165, 188, 200, 245*); and

raising a power supply voltage [*e.g., Fig. 21: at "A"*] of said first latch section from a first voltage [*e.g., Fig. 21: with Qp33 open, first voltage = 0 volts*] to a second voltage [*e.g., Fig. 21:*

with Qp33 closed, second voltage = VDD] while said first latch result is transferred to said second latch section (*e.g., see Fig. 19*);

wherein said second voltage is higher than said first voltage (*e.g., see Fig. 19*), and

wherein said second voltage is a power supply voltage [*e.g., Fig. 26: VDD at 179, "A"*] of said second latching section (*see the entire document, including Paragraphs 176-260*).

Moreover, ***Nakajima*** discloses a data transfer circuit [*e.g., Fig. 1: 123 + 124*] for latching an input data [*e.g., Fig. 30: in1*] in a first latch section [*e.g., Figs. 1: 123; Fig. 30*],

transferring a first latch result [*e.g., Fig. 30: out2 = Fig. 11: in1*] of said first latch section to a second latch section [*e.g., Fig. 1: 124; Fig. 11*], and

latching said first latch result in said second latch section (*e.g., see Fig. 9*), characterized by:

transferring only an inverted [*e.g., Fig. 30: via 190*] output of said first latch result to said second latch section (*e.g., see Paragraphs 147, 165, 188, 200, 245*); and

raising a power supply voltage [*e.g., Fig. 30: at "A"*] of said first latch section from a first voltage [*e.g., Fig. 30: VDD1*] to a second voltage [*e.g., Fig. 30: VDD2*] while said first latch result is transferred to said second latch section; and

wherein said second voltage is higher than said first voltage (*see the entire document, including Paragraphs 135-175 and 210-260*).

Nakajima does not appear to expressly disclose said second voltage [*e.g., Fig. 30: VDD2*] is a power supply voltage [*e.g., Fig. 11: VDD*] of said second latching section.

However, there are only three options in this situation:

1. VDD2 > VDD,

2. VDD2 < VDD, or

3. VDD2 = VDD.

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (*e.g., VDD2 = VDD*). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

Moreover, one having ordinary skill in the art at the time of invention would have obviously recognized the additional benefit of requiring one less power source in the case of "VDD2 = VDD" (*compared with the other two, different power supply options*).

Furthermore, ***Nakajima*** teaches, "*A detailed description of the horizontal registers 121, 131, the* ***sampling & latch circuits 122, 132****, the* ***second latch circuits 123, 133****, the* ***level shifters 124, 134*** *as well as the DA converter circuits 125, 135 was related above. However, the circuit configuration for these embodiments need not all be utilized simultaneously in the respective circuits for the liquid crystal display device and* ***any of these circuits is capable of being utilized in the circuit structure of any of the above embodiments***" (*Paragraph 255*).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use either of ***Nakajima's*** disclosed latch circuits [*e.g., Fig. 30 or Fig. 31*] to form the level shifter [*e.g., Fig. 1: 124*] -- i.e., replacing Figure 11 with either Figure 30 or Figure 31.

Doing so would provide a level shifter structure with only a small number of circuit devices, with no need to rewrite the latch of high voltage amplitude signal with a low voltage amplitude signal so that the size of the signal buffer of the previous stage can be kept small, and a small surface area can be achieved (*e.g., see* ***Nakajima****: Paragraphs 234 and 243*).

Moreover, it would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known *(**Figs. 30 or 31**) latch/level shifter circuit for another (**Fig. 11**) latch/level shifter circuit* would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Similarly, and for the same reasons, it would have been obvious to one having ordinary skill in the art at the time of invention to use either of ***Nakajima's*** disclosed "*second*" latch circuits [*e.g., Fig. 30 or Fig. 31*] to form the "*first*" latch circuit [*e.g., Fig. 1: 122*] -- i.e., replacing Figure 21 with either Figure 30 or Figure 31.

Should it be shown that ***Nakajima*** still discloses a *second latching section*, as instantly claimed, with insufficient specificity:

Azami discloses a data transfer circuit [*e.g., Fig. 18*] for latching an input data [*e.g., Fig. Data In*] in a first latch section [*e.g., Fig. 18: LAT1*],

transferring a first latch result [*e.g., Fig. 18: via 1860*] of said first latch section to a second latch section [*e.g., Fig. 18: LAT2*] (*see the entire document, including Paragraphs 183-186*).

Nakajima and ***Azami*** are analogous art, because they are from the shared inventive field of CMOS latch circuitry for display devices.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Nakajima's*** latch circuitry [*e.g., Fig. 30 or Fig. 31*] to form both of ***Azami's*** latches [*e.g., Fig. 18: LAT1 and LAT2*], so as to provide a latch structure with only a small number of circuit devices, with no need to rewrite the latch of high voltage amplitude signal with a low voltage amplitude signal so that the size of the signal buffer of the previous stage can be kept small, and a small surface area can be achieved (*e.g., see* ***Nakajima****: Paragraphs 234 and 243*).

Moreover, it would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known *(**Nakajima's**) latch circuit for another (**Azami's**) latch circuit* would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Regarding claim 3, ***Nakajima*** discloses said second voltage is sufficiently higher than said first voltage so as to reduce a voltage drop due to a transfer of said first latch to said second latch section by only an inverted output (*e.g., see Paragraphs 176-260*).

Regarding claim 4, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, ***Nakajima*** discloses a data transfer circuit [*e.g., Figs. 1, 23: 122 + 123*] comprising:

a first latch section [*e.g., Figs. 1, 23: 122; Fig. 21*] that latches a data input [*e.g., Fig. 21: in1*] and produces a first latch result [*e.g., Fig. 21: xout = Fig. 26: in1*]; and

a second latch section [*e.g., Figs. 1, 23: 123; Fig. 26*] that latches said first latch result and outputs a transfer circuit output [*e.g., Fig. 26: out2*];

wherein the first latch result is transferred to the second latch section by use of a single phase (*e.g., see Paragraphs 147, 165, 188, 200, 245*),

wherein a power supply voltage [*e.g., Fig. 21: at "A"*] of said first latch section is raised from a first voltage [*e.g., Fig. 21: with Qp33 open, first voltage = 0 volts*] to a second voltage [*e.g., Fig. 21: with Qp33 closed, second voltage = VDD*] while said first latch result is transferred to said second latch section (*e.g., see Fig. 19*), and

wherein said second voltage is higher than said first voltage, and

said second voltage is a power supply voltage [*e.g., Fig. 26: VDD at 179, "A"*] of said second latching section (*see the entire document, including Paragraphs 176-260*).

Moreover, ***Nakajima*** discloses a data transfer circuit [*e.g., Fig. 1: 123 + 124*] comprising:

a first latch section [*e.g., Figs. 1: 123; Fig. 30*] that latches a data input [*e.g., Fig. 30: in1*] and produces a first latch result [*e.g., Fig. 30: out2 = Fig. 11: in1*]; and

a second latch section [*e.g., Fig. 1: 124; Fig. 11*] that latches said first latch result and outputs a transfer circuit output [*e.g., Fig. 11: xout*];

wherein the first latch result is transferred to the second latch section by use of a single phase (*e.g., see Paragraphs 147, 165, 188, 200, 245*),

wherein a power supply voltage [*e.g., Fig. 30: at "A"*] of said first latch section is raised from a first voltage [*e.g., Fig. 30: VDD1*] to a second voltage [*e.g., Fig. 30: VDD2*] while said first latch result is transferred to said second latch section, and

wherein said second voltage is higher than said first voltage (*see the entire document, including Paragraphs 135-175 and 210-260*).

Nakajima does not appear to expressly disclose said second voltage [*e.g., Fig. 30: VDD2*] is a power supply voltage [*e.g., Fig. 11: VDD*] of said second latching section.

However, there are only three options in this situation:

1. VDD2 > VDD,

2. VDD2 < VDD, or

3. VDD2 = VDD.

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (*e.g., VDD2 = VDD*). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

Moreover, one having ordinary skill in the art at the time of invention would have obviously recognized the additional benefit of requiring one less power source in the case of "VDD2 = VDD" (*compared with the other two, different power supply options*).

Furthermore, ***Nakajima*** teaches, "*A detailed description of the horizontal registers 121, 131, the* ***sampling & latch circuits 122, 132****, the* ***second latch circuits 123, 133****, the* ***level shifters 124, 134*** *as well as the DA converter circuits 125, 135 was related above. However, the circuit configuration for these embodiments need not all be utilized simultaneously in the respective circuits for the liquid crystal display device and* ***any of these circuits is capable of being utilized in the circuit structure of any of the above embodiments***" (*Paragraph 255*).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use either of ***Nakajima's*** disclosed latch circuits [*e.g., Fig. 30 or Fig. 31*] to form the level shifter [*e.g., Fig. 1: 124*] -- i.e., replacing Figure 11 with either Figure 30 or Figure 31.

Doing so would provide a level shifter structure with only a small number of circuit devices, with no need to rewrite the latch of high voltage amplitude signal with a low voltage amplitude signal so that the size of the signal buffer of the previous stage can be kept small, and a small surface area can be achieved (*e.g., see* ***Nakajima****: Paragraphs 234 and 243*).

Moreover, it would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known *(**Figs. 30 or 31**) latch/level shifter circuit for another (**Fig. 11**) latch/level shifter circuit* would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Similarly, and for the same reasons, it would have been obvious to one having ordinary skill in the art at the time of invention to use either of ***Nakajima's*** disclosed "*second*" latch

circuits [*e.g., Fig. 30 or Fig. 31*] to form the "*first*" latch circuit [*e.g., Fig. 1: 122*] -- i.e., replacing Figure 21 with either Figure 30 or Figure 31.

Should it be shown that ***Nakajima*** still discloses a *second latching section*, as instantly claimed, with insufficient specificity:

Azami discloses a data transfer circuit [*e.g., Fig. 18*] comprising:

a first latch section [*e.g., Fig. 18: LAT1*] that latches a data input [*e.g., Fig. Data In*] and produces a first latch result [*e.g., Fig. 18: at 1860*]; and

a second latch section [*e.g., Fig. 18: LAT2*] that latches said first latch result and outputs a transfer circuit output [*e.g., Fig. 18: Data Out*];

wherein the first latch result is transferred to the second latch section by use of a single phase (*see the entire document, including Paragraphs 183-186*).

Nakajima and ***Azami*** are analogous art, because they are from the shared inventive field of CMOS latch circuitry for display devices.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Nakajima's*** latch circuitry [*e.g., Fig. 30 or Fig. 31*] to form both of ***Azami's*** latches [*e.g., Fig. 18: LAT1 and LAT2*], so as to provide a latch structure with only a small number of circuit devices, with no need to rewrite the latch of high voltage amplitude signal with a low voltage amplitude signal so that the size of the signal buffer of the previous stage can be kept small, and a small surface area can be achieved (*e.g., see **Nakajima**: Paragraphs 234 and 243*).

Moreover, it would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known *(**Nakajima's**) latch circuit for another (**Azami's**) latch circuit* would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Regarding claim 7, ***Nakajima*** discloses said second voltage is sufficiently higher than said first voltage so as to reduce a voltage drop due to the transfer of said first latch result to said second latch section (*e.g., see Paragraphs 176-260*).

Regarding claim 10, ***Nakajima*** discloses said data input is gradation data (*e.g., see Paragraphs 105-125*).

Regarding claim 6, ***Nakajima*** discloses said transfer by use of a single phase is carried out by use of a non-inverted output of the first latch result [*e.g., Fig. 21: out = Fig. 26: in2*] (*e.g., see Paragraphs 147, 165, 188, 200, 245*).

Moreover, ***Nakajima*** discloses said transfer by use of a single phase is carried out by use of a non-inverted output of the first latch result [*e.g., Fig. 30: out1 = Fig. 11: in2*] (*e.g., see Paragraphs 147, 165, 188, 200, 245*).

Regarding claim 9, ***Nakajima*** discloses said second voltage is sufficiently higher than said first voltage so as to reduce a voltage drop due to the transfer of said first latch result to said second latch section (*e.g., see Paragraphs 176-260*).

Regarding claim 5, ***Nakajima*** discloses said transfer by use of a single phase is carried out by use of an inverted [*e.g., Fig. 21: via 114; Fig. 30: via 190*] output of the first latch result (*e.g., see Paragraphs 147, 165, 188, 200, 245*).

Regarding claim 8, ***Nakajima*** discloses said second voltage is sufficiently higher than said first voltage so as to reduce a voltage drop due to the transfer of said first latch result to said second latch section (*e.g., see Paragraphs 176-260*).

Regarding claim 15, ***Nakajima*** discloses said second latch section [*e.g., Figs. 1, 23: 123; Fig. 26*] further comprises

a third inverter [*e.g., Fig. 26: 171*] and

a fourth inverted [*e.g., Fig. 26: via 172*],

said third and fourth inverters [*e.g., Fig. 26: 172*] arranged in parallel between said power supply voltage maintained at said second voltage and a second negative power supply [*e.g., Fig. 26: VSS1, VSS2*];

wherein said first latch result is inputted to said third inverter and the output of said third inverter is inputted to said fourth inverter (*e.g., see Paragraphs 176-260*).

Moreover, ***Nakajima*** discloses said second latch section [*e.g., Fig. 1: 124; Fig. 11*] further comprises

a third inverter [*e.g., Fig. 11: 71*] and

a fourth inverted [*e.g., Fig. 11: via 72*],

said third and fourth inverters [*e.g., Fig. 11: 72*] arranged in parallel between said power supply voltage maintained at said second voltage and a second negative power supply [*e.g., Fig. 11: GND*];

wherein said first latch result is inputted to said third inverter and the output of said third inverter is inputted to said fourth inverter (*e.g., see Paragraphs 135-175 and 210-260*).

Regarding claim 14, ***Nakajima*** discloses a transfer switch [*e.g., Fig. 26: 175*] is arranged between said first latch section [*e.g., Figs. 1, 23: 122; Fig. 21*] and said second latch section [*e.g., Figs. 1, 23: 123; Fig. 26*],

an output of said transfer switch being supplied to said second latch section (*e.g., see Paragraphs 176-260*).

Moreover, ***Nakajima*** discloses a transfer switch [*e.g., Fig. 11: Qn13*] is arranged between said first latch section [*e.g., Figs. 1: 123; Fig. 30*] and said second latch section [*e.g., Fig. 1: 124; Fig. 11*],

an output of said transfer switch being supplied to said second latch section (*e.g., see Paragraphs 135-175 and 210-260*).

Regarding claim 16, ***Nakajima*** discloses said second latch section [*e.g., Figs. 1, 23: 123; Fig. 26*] level shifts said transfer circuit [*e.g., Fig. 26: 175*] output by setting-up said second negative power supply [*e.g., Fig. 26: VSS1, VSS2*] (*e.g., see Paragraphs 176-260*).

Moreover, ***Nakajima*** discloses said second latch section [*e.g., Fig. 1: 124; Fig. 11*] level shifts said transfer circuit [*e.g., Fig. 11: Qn13*] output by setting-up said second negative power supply [*e.g., Fig. 11: GND*] (*e.g., see Paragraphs 135-175 and 210-260*).

Regarding claim 11, ***Nakajima*** discloses said first latch section [*e.g., Figs. 1, 23: 122; Fig. 21*] further comprises

a first inverter [*e.g., Fig. 21: 101*] and

a second inverted [*e.g., Fig. 21: via 102*],

said first and second inverters [*e.g., Fig. 21: 102*] arranged in parallel between said power supply voltage and a first negative power supply [*e.g., Fig. 21: GND*];

wherein said data input is inputted to said first inverter (*e.g., see Paragraphs 176-260*).

Moreover, ***Nakajima*** discloses said first latch section [*e.g., Figs. 1: 123; Fig. 30; Fig. 31*] further comprises

a first inverter [*e.g., Fig. 30: 191; Fig. 31: 211*] and

a second inverted [*e.g., Fig. 30: via 192; Fig. 31: via 212*],

said first and second inverters [*e.g., Fig. 30: 192; Fig. 31: 212*] arranged in parallel between said power supply voltage and a first negative power supply [*e.g., Fig. 30: VSS; Fig. 31: VSS1, VSS2*];

wherein said data input is inputted to said first inverter (*e.g., see Paragraphs 135-175 and 210-260*).

Regarding claim 12, ***Nakajima*** discloses an output from said first inverter [*e.g., Fig. 21: 101*] is inputted to said second inverter [*e.g., Fig. 21: 102*] via a switching circuit [*e.g., Fig. 21: Qp33*] that operates off-action at a sampling pulse [*e.g., Fig. 21: SP*] (*e.g., see Paragraphs 176-260*).

Moreover, ***Nakajima*** discloses an output from said first inverter [*e.g., Fig. 30: 191; Fig. 31: 211*] is inputted to said second inverter [*e.g., Fig. 30: 192; Fig. 31: 212*] via a switching circuit [*e.g., Fig. 30: 200; Fig. 31: 220*] that operates off-action at a sampling pulse [*e.g., Fig. 30: oe2; Fig. 31: oe2*] (*e.g., see Paragraphs 135-175 and 210-260*).

Regarding claim 13, ***Nakajima*** discloses said data input is inputted to said first inverter [*e.g., Fig. 21: 101*] via a transistor [*e.g., Fig. 21: Qn33*] which operates on-action at said sampling pulse (*e.g., see Paragraphs 176-260*).

Moreover, ***Nakajima*** discloses said data input is inputted to said first inverter [*e.g., Fig. 30: 191; Fig. 31: 211*] via a transistor [*e.g., Fig. 30: 195; Fig. 31: 215*] which operates on-action at said sampling pulse (*e.g., see Paragraphs 135-175 and 210-260*).

43. *Claims 12 and 13* are further rejected under 35 U.S.C. 103(a) as being unpatentable over ***Nakajima et al (EP 1 014 334 A2)*** and ***Azami et al (US 2003/0011584 A1)*** as applied to *claim 11* above, and further in view of the instant application's ***Admitted Prior Art (APA)***.

Regarding claims 12 and 13, should it be shown that the combination of ***Nakajima*** and ***Azami*** discloses a *switching circuit*, as instantly claimed, with insufficient specificity:

The ***APA*** discloses a data transfer circuit [*e.g., Fig. 2*] comprising:

a first latch section [*e.g., Fig. 2: 21*] that latches a data input [*e.g., Fig. 2: D1*] and produces a first latch result [*e.g., Fig. 2: 1Lout$_{(inv)}$*]; and

a second latch section [*e.g., Fig. 2: 22*] that latches said first latch result and outputs a transfer circuit output [*e.g., Fig. 2: 2Lout*];

wherein the first latch result is transferred to the second latch section by use of a single phase [*e.g., Fig. 2: 1Lout$_{(inv)}$ is a "single phase"*],

wherein a power supply voltage [*e.g., Fig. 2: VCC = 2.9V*] of said first latch section is a power supply voltage [*e.g., Fig. 2: VH = 2.9V*] of said second latching section;

said transfer by use of a single phase is carried out by use of an inverted [*e.g., Fig. 2: via 24*] output of the first latch result;

said first latch section further comprises

a first inverter [*e.g., Fig. 2: Q1, Q2*] and

a second inverted [*e.g., Fig. 2: via Q3, Q4*],

said first and second inverters [*e.g., Fig. 2: Q3, Q4*] arranged in parallel between said power supply voltage and a first negative power supply [*e.g., Fig. 2: VSS*];

wherein said data input is inputted to said first inverter;

an output from said first inverter is inputted to said second inverter via a switching circuit [*e.g., Fig. 2: Q5*] that operates off-action at a sampling pulse [*e.g., Fig. 2: xSP*];

said data input is inputted to said first inverter via a transistor [*e.g., Fig. 2: Q6*] which operates on-action at said sampling pulse

(*see the entire **APA**, including Figs. 1-3; Page 1, Line 20 - Page 6, Line 27*).

Nakajima, ***Azami***, and the ***APA*** are analogous art, because they are from the shared inventive field of CMOS latch circuitry for display devices.

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to use ***Nakajima's*** latch circuitry [*e.g., Fig. 30 or Fig. 31*] to form both of the ***APA's*** latches [*e.g., Fig. 2: 21, 22*], so as to provide a latch structure with only a small number of circuit devices, with no need to rewrite the latch of high voltage amplitude signal with a low voltage amplitude signal so that the size of the signal buffer of the previous stage can be kept small, and a small surface area can be achieved (*e.g., see **Nakajima**: Paragraphs 234 and 243*).

Moreover, it would have been obvious to one of ordinary skill in the art at the time of invention, because the substitution of one known *(**Nakajima's**) latch circuit for another (the*

APA's) *latch circuit* would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Furthermore, it would have been obvious to one having ordinary skill in the art at the time of invention to use the ***APA's*** switching circuit arrangement [*e.g., Fig. 2: Q5*] to form ***Nakajima*** and ***Azami's*** combined first latch sections, so as to provide additional timing control over the resultant latches (*e.g., see the* ***APA****: Page 5, Lines 14-28*).

Lastly, it would have been obvious to one of ordinary skill in the art at the time of invention because all the claimed elements were known in the prior art and one skilled in the art could have combined *the* ***APA's*** *switching circuit arrangement with* ***Nakajima*** *and* ***Azami's*** *combined first latch sections* as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Response to Arguments

44. Applicant's arguments filed on *4 November 2009* have been fully considered but they are not persuasive.

Applicant's arguments with respect to *claims 1, 3, 4, 5, 7, 8, and 10-16* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

45. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
21 May 2010